



VND5012AK-E

DOUBLE CHANNEL HIGH SIDE DRIVER WITH ANALOG CURRENT SENSE FOR AUTOMOTIVE APPLICATIONS

ADVANCE DATA

Table 1. General Features

TYPE	V _{CC}	R _{DS(on)}	I _D
VND5012AK-E	41V	12mΩ (*)	40A

(*) Per channel

- OUTPUT CURRENT: 40A
- 3.0V CMOS COMPATIBLE INPUT
- CURRENT SENSE DISABLE
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT AND POWER LIMITATION
- VERY LOW STAND-BY CURRENT
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V_{CC}
- VERY LOW ELECTROMAGNETIC SUSCEPTIBILITY
- OPTIMIZED ELECTROMAGNETIC EMISSION
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

DESCRIPTION

The VND5012AK-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VND5012AK-E	VND5012AKTR-E

Note: (**) See application schematic at page 8

Figure 2. Block Diagram

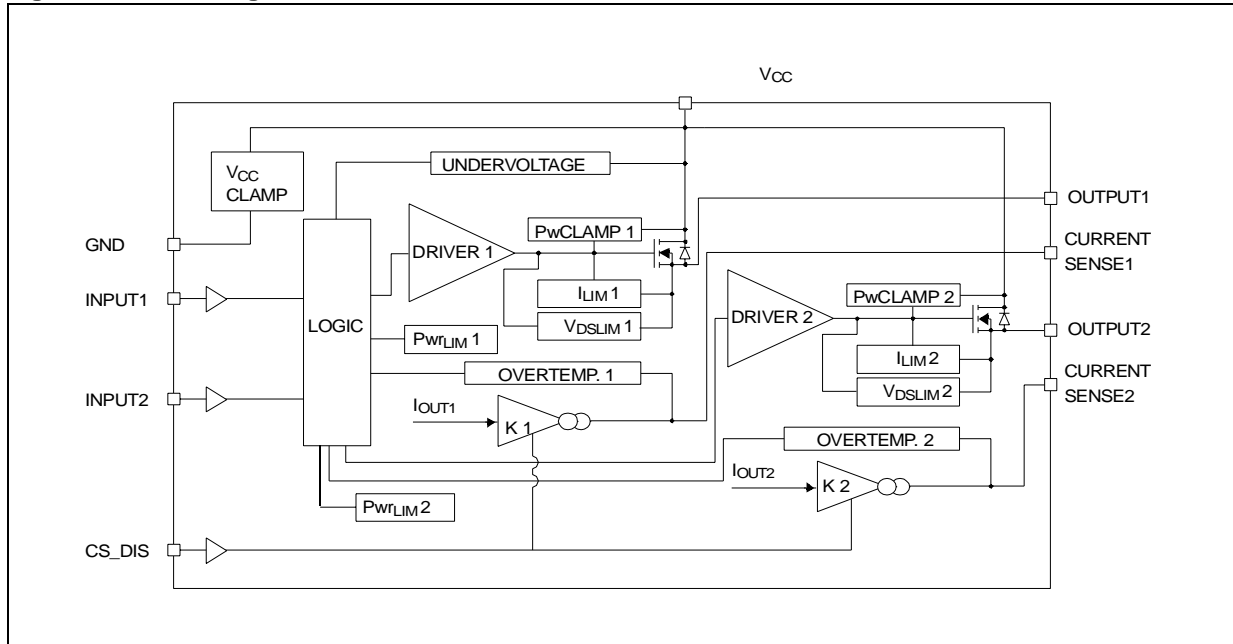


Table 3. Pin Function

Name	Function
V _{CC}	Battery connection
OUTPUT _{1,2}	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE _{1,2}	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 3. Current and Voltage Conventions

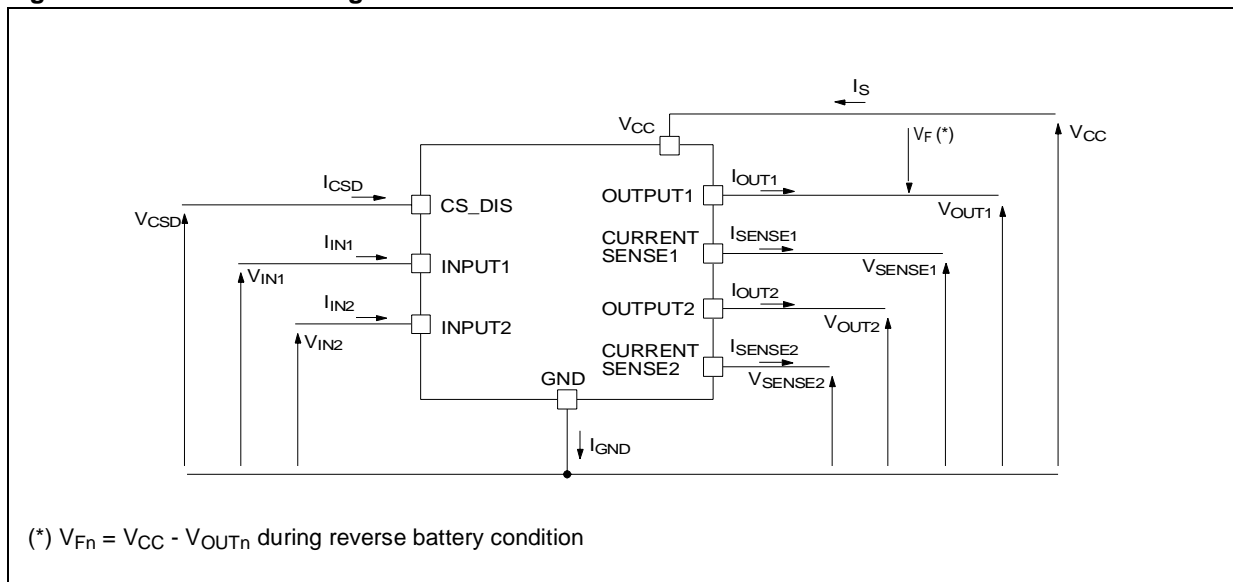
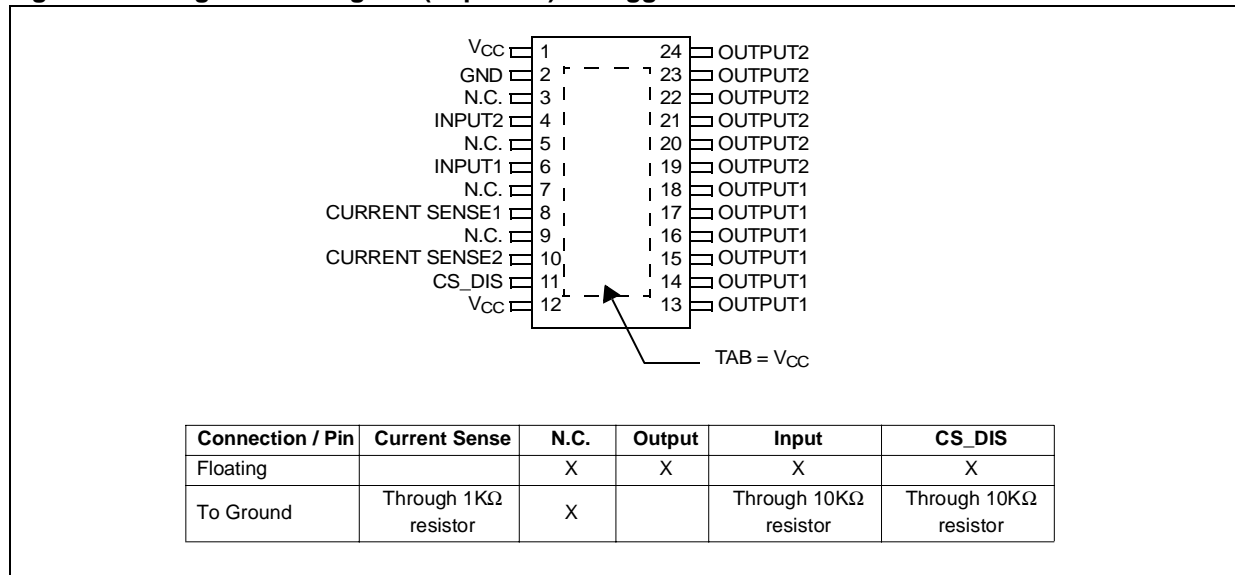


Figure 4. Configuration Diagram (Top View) & Suggested Connections For Unused and n.c. Pins**Table 4. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-30	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$V_{CSSENSE}$	Current sense maximum voltage	$V_{CC}-41$ $+V_{CC}$	V V
V_{ESD}	Electrostatic discharge ($R=1.5k\Omega$; $C=100pF$)	2000	V
T_j	Junction operating temperature	-40 to 150	$^{\circ}C$
T_{stg}	Storage temperature	-55 to 150	$^{\circ}C$

Table 5. Thermal Data

Symbol	Parameter	Max Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.7	$^{\circ}C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	52 (see note 1)	$^{\circ}C/W$

Note: 1. When mounted on a standard single-sided FR4 board with 1cm² of Cu (at least 35 μ m thick) connected to TAB.

ELECTRICAL CHARACTERISTICS ($8V < V_{CC} < 36V$; $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise specified)

Table 6. Power Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	36	V
V_{USD}	Undervoltage shutdown			3	4.5	V
$V_{USDhyst}$	Undervoltage shut-down hysteresis			0.5		V
R_{ON}	On state resistance	$I_{OUT}=5A$; $T_j=25^{\circ}C$			12	m Ω
		$I_{OUT}=5A$; $T_j=150^{\circ}C$			24	m Ω
		$I_{OUT}=5A$; $V_{CC}=5V$; $T_j=25^{\circ}C$			16	m Ω
V_{clamp}	Clamp Voltage	$I_S=20\text{ mA}$	41	46	52	V
I_S	Supply current	Off State; $V_{CC}=13V$; $T_j=25^{\circ}C$; $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V$		2(**)	5(**)	μA
		On State; $V_{CC}=13V$; $V_{IN}=5V$; $I_{OUT}=0A$		3	6	mA
$I_{L(off)}$	Off state output current	$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=25^{\circ}C$	0		3	μA
		$V_{IN}=V_{OUT}=0V$; $V_{CC}=13V$; $T_j=125^{\circ}C$	0		5	

Note: (**) PowerMOS leakage included

Table 7. Switching ($V_{CC}=13V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=2.6\Omega$		15		μs
$t_{d(off)}$	Turn-off delay time	$R_L=2.6\Omega$		40		μs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L=2.6\Omega$		0.3		V/ μs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L=2.6\Omega$		0.35		V/ μs
W_{ON}	Switching energy losses at turn-on	$R_L=2.6\Omega$		TBD		mJ
W_{OFF}	Switching energy losses at turn-off	$R_L=2.6\Omega$		TBD		mJ

ELECTRICAL CHARACTERISTICS (continued)**Table 8. Logic Input**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} =0.9 V	1			μA
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{I(hyst)}	Input hysteresis voltage		0.25			V
V _{ICL}	Input clamp voltage	I _{IN} =1mA I _{IN} =-1mA	5.5	-0.7	TBD	V V
V _{CSDL}	CS_DIS low level voltage				0.9	V
I _{CSDL}	Low level CS_DIS current	V _{CSD} = 0.9V	1			μA
V _{CSDH}	CS_DIS high level voltage		2.1			V
I _{CSDH}	High level CS_DIS current	V _{CSD} = 2.1 V			10	μA
V _{CSD(hyst)}	CS_DIS hysteresis voltage		0.25			V
V _{C_SCL}	CS_DIS clamp voltage	I _{CSD} =1mA I _{CSD} =-1mA	5.5	-0.7	TBD	V V

Table 9. Protections and Diagnostics (see note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I _{limH}	DC Short circuit current	V _{CC} =13V 5V<V _{CC} <36V	40	60	80 80	A A
I _{limL}	Short circuit current during thermal cycling	V _{CC} =13V; T _R <T _j <T _{TSD}		24		A
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		T _{RS} + 1	T _{RS} + 5		°C
T _{RS}	Thermal reset of STATUS		135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R)			7		°C
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} =2A; V _{IN} =0; L=6mH	V _{CC} -41	V _{CC} -46	V _{CC} -52	V
V _{ON}	Output voltage drop limitation	I _{OUT} =0.4A T _j = -40°C...+150°C (see fig. 9)		25		mV

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

ELECTRICAL CHARACTERISTICS (continued)

Table 10. Current Sense ($8V < V_{CC} < 16V$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} =1.5A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C...150°C	TBD	5000	TBD	
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} =10A; V _{SENSE} =4V; V _{CSD} =0V; T _j =-40°C T _j =25°C...150°C	TBD	5000	TBD	
			TBD	5000	TBD	
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} =25A; V _{SENSE} =4V; V _{CSD} =0V; T _j =-40°C T _j =25°C...150°C	TBD	5000	TBD	
			TBD	5000	TBD	
I _{SENSE0}	Analog sense current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _j =-40°C...150°C V _{CSD} =0V; V _{IN} =5V; T _j =-40°C...150°C	0		5	μA
			0		10	μA
V _{SENSE}	Max analog sense output voltage	I _{OUT} =15A; V _{CSD} =0V; R _{SENSE} =3.9KΩ	5			V
V _{SENSEH}	Analog sense output voltage in overtemperature condition	V _{CC} =13V; R _{SENSE} =3.9KΩ		9		V
I _{SENSEH}	Analog sense output current in overtemperature condition	V _{CC} =13V		8		mA
t _{DSENSE1H}	Delay Response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE max} (see fig 5)		50	100	μs
t _{DSENSE1L}	Delay Response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =10% of I _{SENSE max} (see fig 5)		5	20	μs
t _{DSENSE2H}	Delay Response time from rising edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =90% of I _{SENSE max} (see fig 5)		270	600	μs
t _{DSENSE2L}	Delay Response time from falling edge of INPUT pin	V _{SENSE} <4V, 1.5A<I _{OUT} <25A I _{SENSE} =10% of I _{SENSE max} (see fig 5)		100	250	μs

Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE (V _{CSD} =0V) (see note 3)
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V _{SENSEH}
Undervoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	0
Short circuit to V _{CC}	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Note: 3. If the V_{CSD} is high, the SENSE output is at a high impedance.

Figure 5.

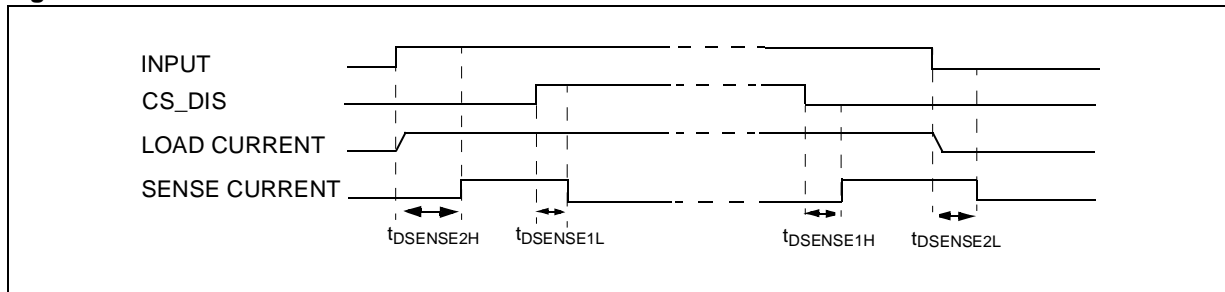


Figure 6.

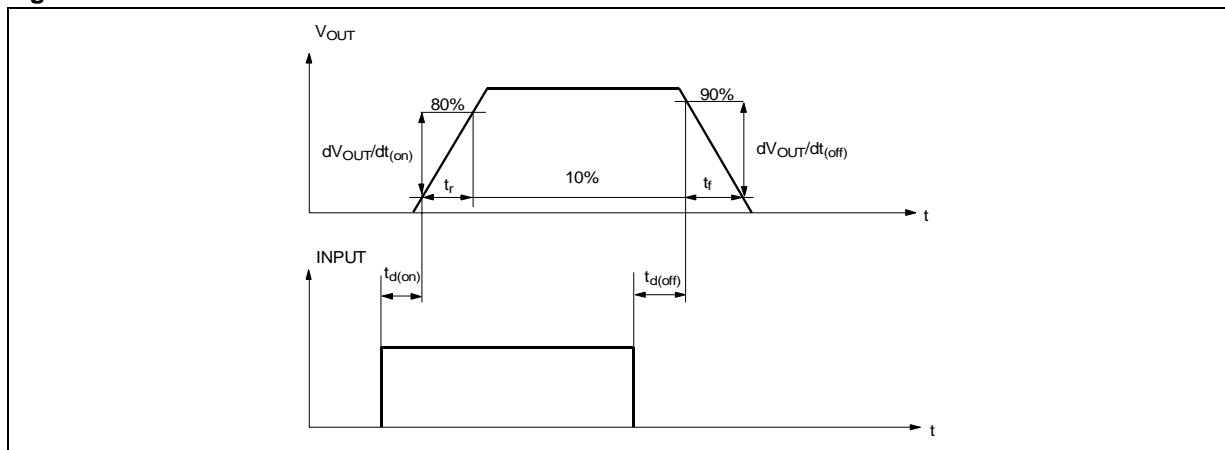


Table 12. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μ s 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μ s 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Application Schematic

GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1) $R_{GND} \leq 600\text{mV} / (I_{S(ON)max})$.
- 2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should

Figure 8. Waveforms

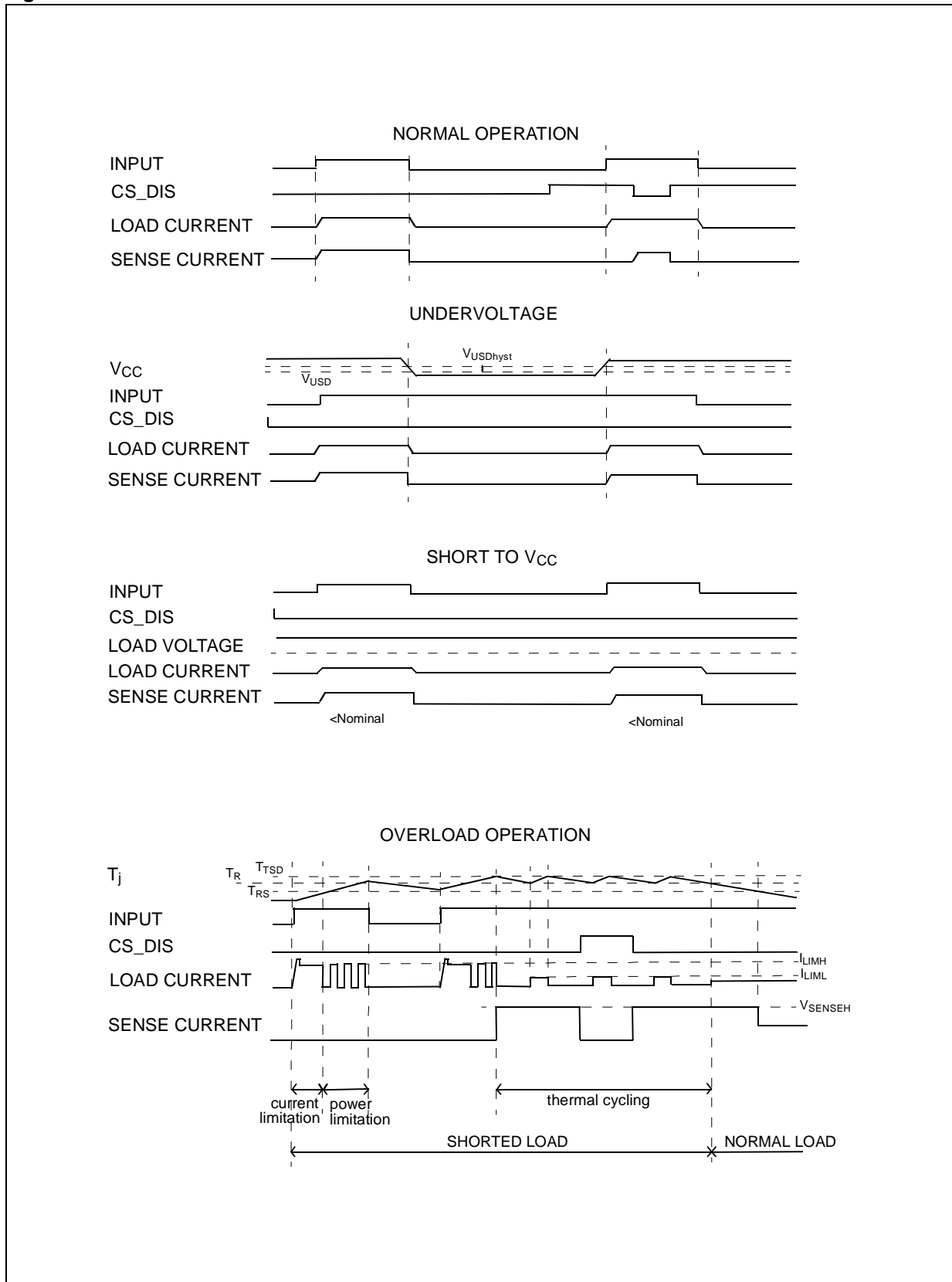
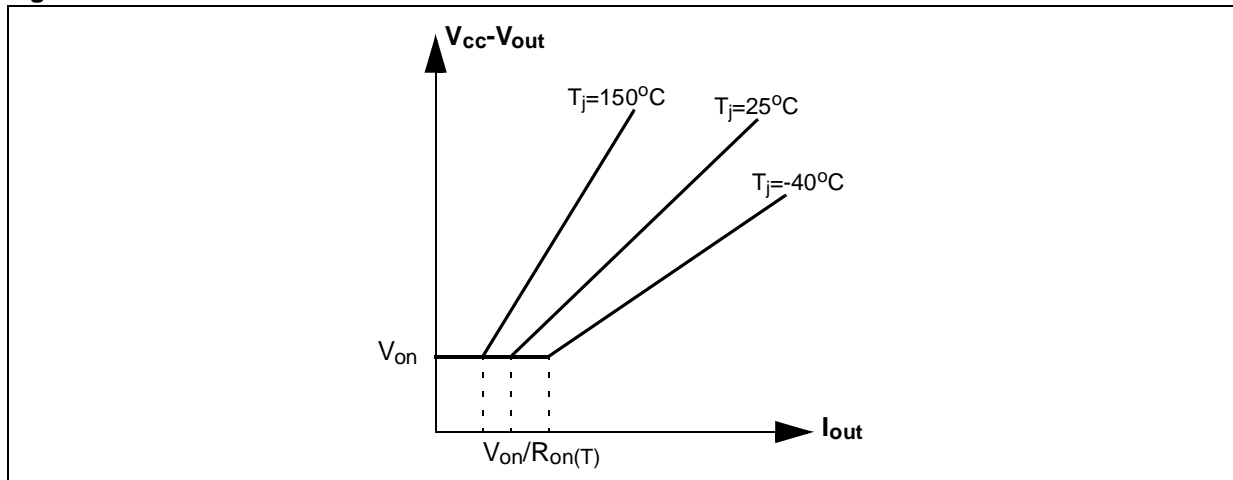


Figure 9.

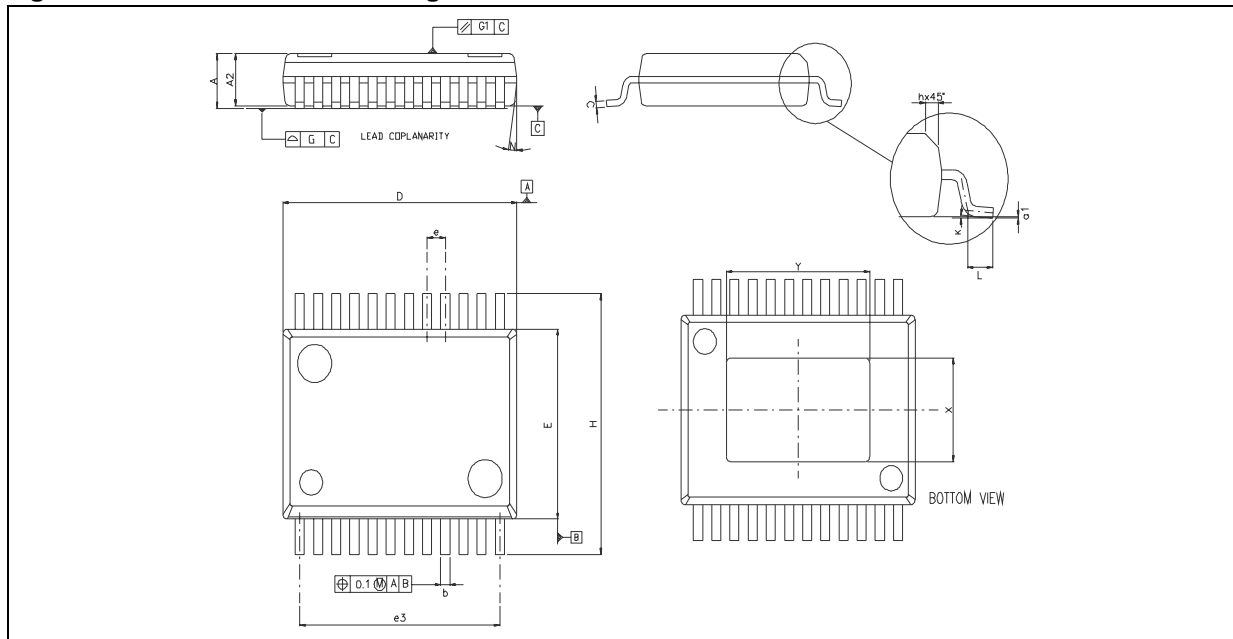


PACKAGE MECHANICAL

Table 13. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	1.9		2.22
A2	1.9		2.15
a1	0		0.07
b	0.34	0.4	0.46
c	0.23		0.32
D	10.2		10.4
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10°
X	3.9		4.3
Y	6.1		6.5

Figure 10. PowerSSO-24™ Package Dimensions



REVISION HISTORY

Table 14. Revision History

Date	Revision	Description of Changes
Sep. 2004	1	- First issue.
Oct. 2004	2	- Minor text changes.
Jan. 2005	3	- Minor text changes.

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