VND5025LAK-E

Features

		41
		4.5 36
		25 Ω
		60
		2μ (1)

1.

■ 3.0

2002/ 5/

■

■


-24

Description

5025 0-5

7637

Table 1. Order codes

Package	Tube	Tape and Reel
-24	5025 -	5025 -

Figure 26: Application schematic

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

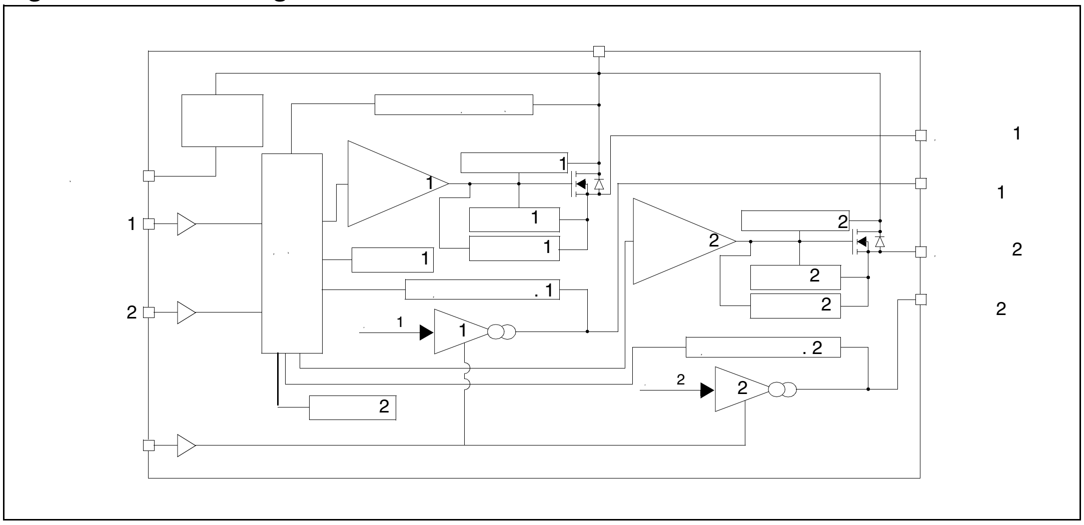
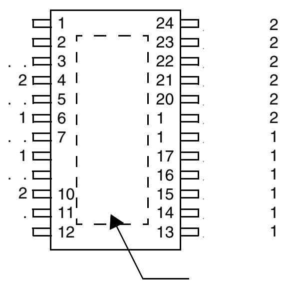


Table 2. Pin functions

Name	Function
[illegible]	[illegible]
[illegible] 1,2	[illegible]
[illegible]	[illegible]
[illegible] 1,2	[illegible]
[illegible] 1,2	[illegible]
[illegible]	[illegible]

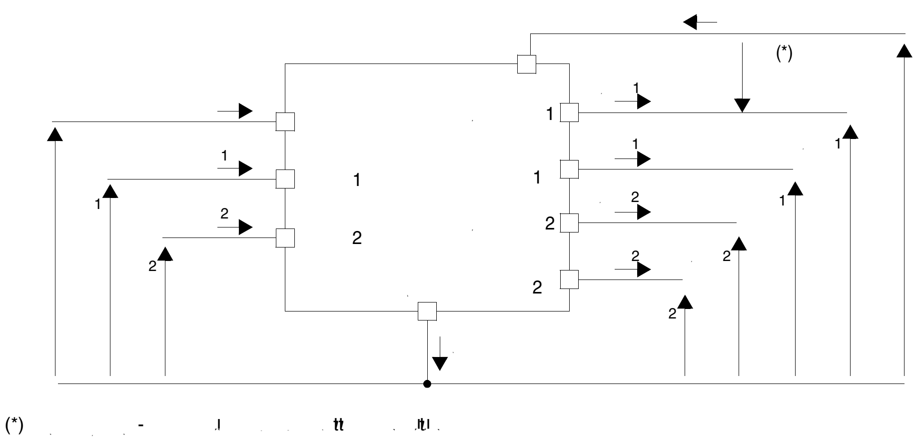
Figure 2. Configuration diagram (top view) and suggested connections for unused and N.C. pins



Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
[illegible]	[illegible]				
[illegible]	1. Ω [illegible]		[illegible]	10 Ω [illegible]	10 Ω [illegible]

2 Electrical characteristics

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
		41	
		0.3	
		200	
		24	
		-1 10	
		200	
		- 41 +	
(1)	( ) (0.3 , 0Ω, 13.5 , 150 , (Typ.))	10	
	(1.5 Ω, 100) - - - - -	 4000 2000 4000 5000 5000	
	(- - 100-011)	750	
		-40 150	
		-55 150	

1. *Section 3.4*

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max Value	Unit
	- ( ) ( )	1.35	/
	- ( )	*Figure 29*	

Table 5. Power section (8V < V_{CC} < 36V; -40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
			4.5	13	36	
				3.5	4.5	
				0.5		
	(1)	3 , 25			25	Ω
		3 , 150			50	
		3 , 5 , 25			35	
		20	41	46	52	
		13 , 25 , 0		2 (2)	5 (2)	µ
		13 , 5 , 0		3	6	
( )	(1)	0 , 13 , 25	0	0.01	3	µ
		0 , 13 , 125	0		5	
	(1)	- 4 , 150			0.7	

1.

2.

Table 6. Switching (V_{CC} = 13V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
( )		4.3Ω (*Figure 8*)		35		µ
( )				50		
(/)		4.3Ω		(*Figure 21*)		/µ
(/)				(*Figure 22*)		
		4.3Ω (*Figure 8*)		0.45		
				0.35		

Table 7. Logic input

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
					0.	
		0.	1			μ
			2.1			
		2.1			10	μ
			0.25			
		1	5.5		7	
		-1		-0.7		
					0.	
		0.	1			μ
			2.1			
		2.1			10	μ
			0.25			
		1	5.5		7	
		-1		-0.7		

Table 8. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
		13	43	60	5	
		5 36				
		13 ,		24		
			150	175	200	
			+ 1	+ 5		
			135			
	(-)			7		
	-	2 , 0, 6	- 41	- 46	- 52	
		0.2 , -40 +150 (*Figure 9*)		40		

1.

Table 9. Current sense (8V < V_{CC} < 16V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
	/	0.05 , 0.5 , 0 , J -40 t 150	1450	3300	51 0	
0	/	0.5 , 0.5 , 0 , J -40 t 150	1720	3020	4360	
1	/	2 , 4 , 0 , J -40 J 25 t 150	1 40 2230	2 10 2 10	3740 33 0	
1/ 1(1)	t tl lt	2 , 4 , 0 , J -40 t 150	-10		+10	%
2	/	3 , 4 , 0 , J -40 J 25 t 150	2250 2400	27 0 27 0	3450 31 0	
2/ 2(1)	t tl lt	3 , 4 , 0 , J -40 t 150	-7		+7	%
3	/	10 , 4 , 0 , J -40 J 25 t 150	2610 2650	2760 2760	2 70 2 70	
3/ 3(1)	t tl lt	10 , 4 , 0 , J -40 t 150	-3		+3	%
0	t	0 , 0 , 5 , 0 , J -40 t 150 0 , 5 , J -40 t 150 2 , 0 , 5 , 5 , J -40 t 150	0 0 0		1 2 1	µ µ µ
	t t t	3 , 0	5			
	t t t l t t ltl	13 , 3. . Ω				
	t t t l t t ltl	13 , 5				

Table 9. Current sense (8V < V_{CC} < 16V) (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t 1	tI .I .I	4 , 0.5 10 0% (*Figure 4*)		50	100	
t 1	tI .I .I .I	4 , 0.5 10 10% (*Figure 4*)		5	20	
t 2	tI .I .I .I	4 , 0.5 10 0% (*Figure 4*)		70	300	µ
Δt 2	tI t .I .I t t t .I .I t	4 , 0% 0% , 3 (*Figure 5*)			110	
t 2	tI .I .I	4 , 0.5 10 10% (*Figure 4*)		100	250	

1. t t .I , .t.I tt t .

Figure 4. Current sense delay characteristics

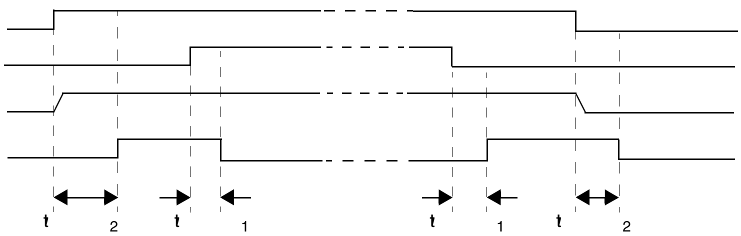


Figure 5. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

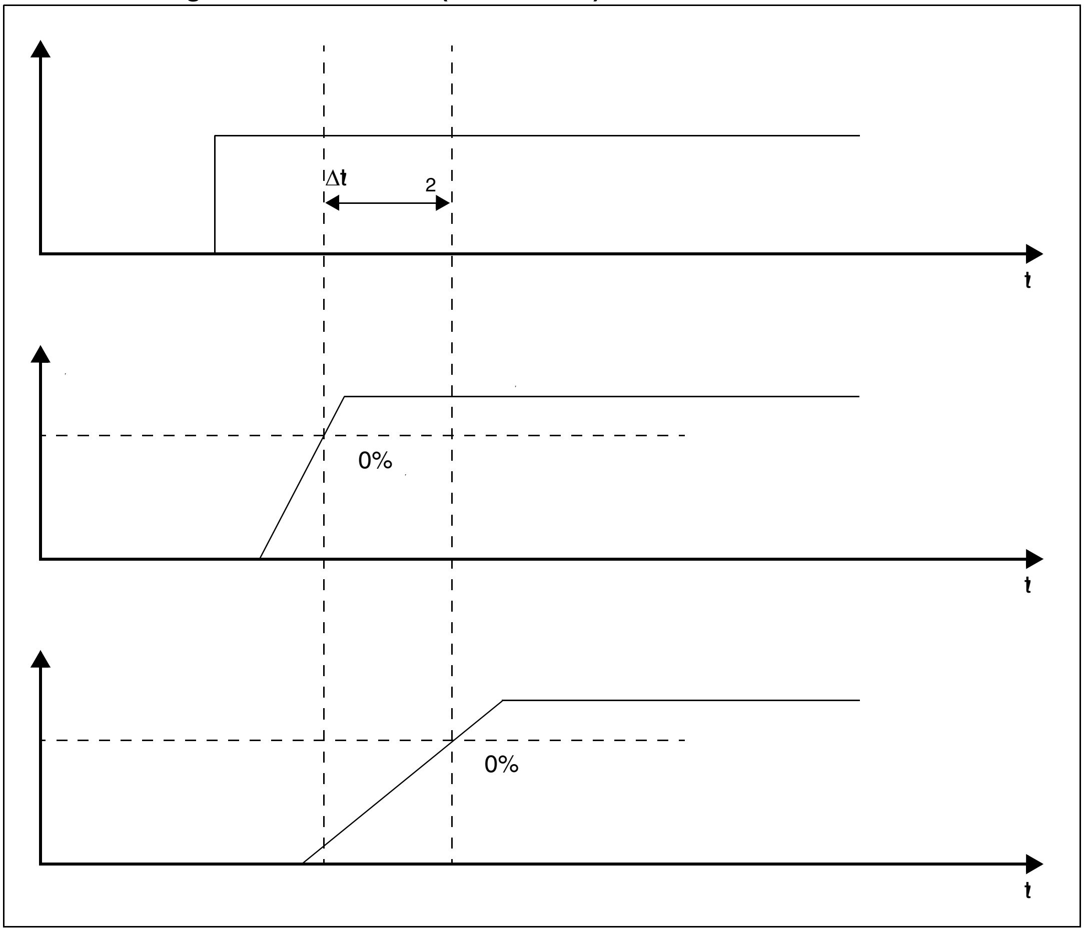


Figure 6. I_{OUT}/I_{SENSE} **vs** I_{OUT} (*Table 9* t .I.)

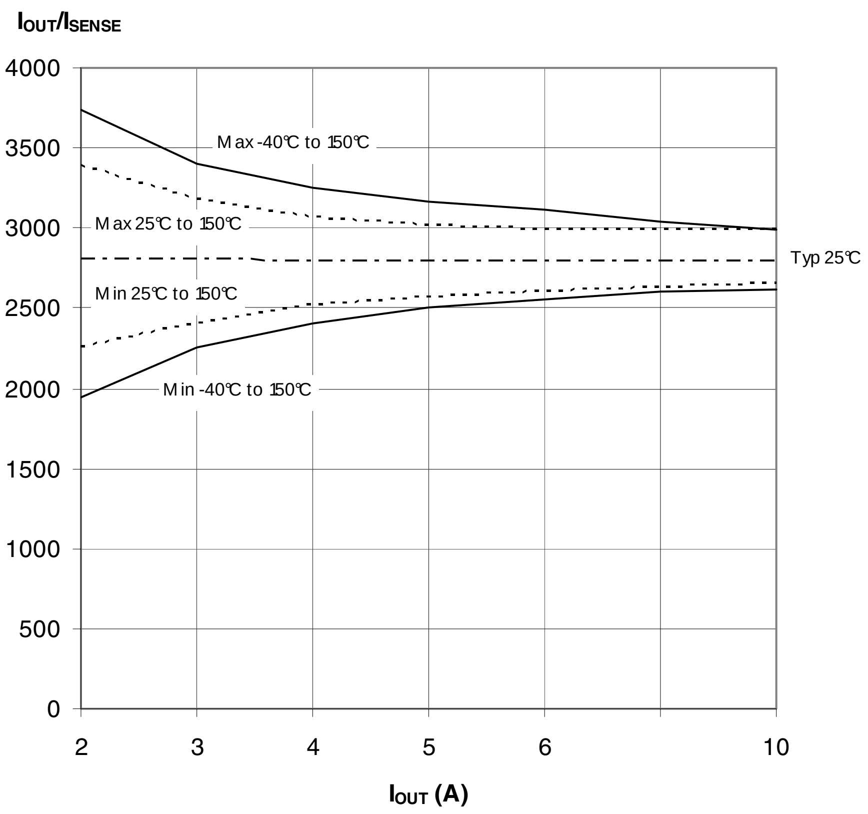


Figure 7. Maximum current sense ratio drift vs load current

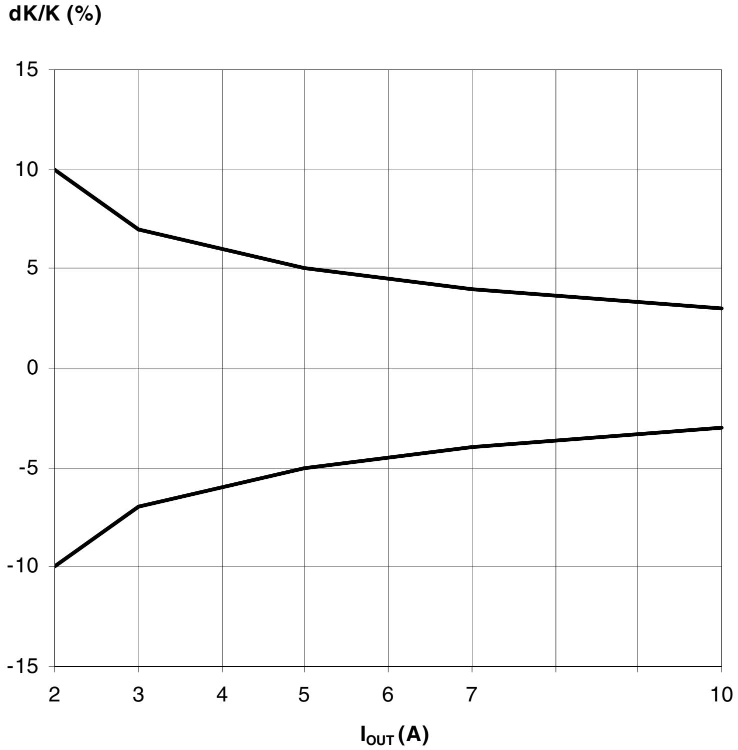


Table 10. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0V)[(1)]
			0
			0
			0
(≤ 10 Ω)			0
			0
			0
			0

1.

Figure 8. Switching characteristics

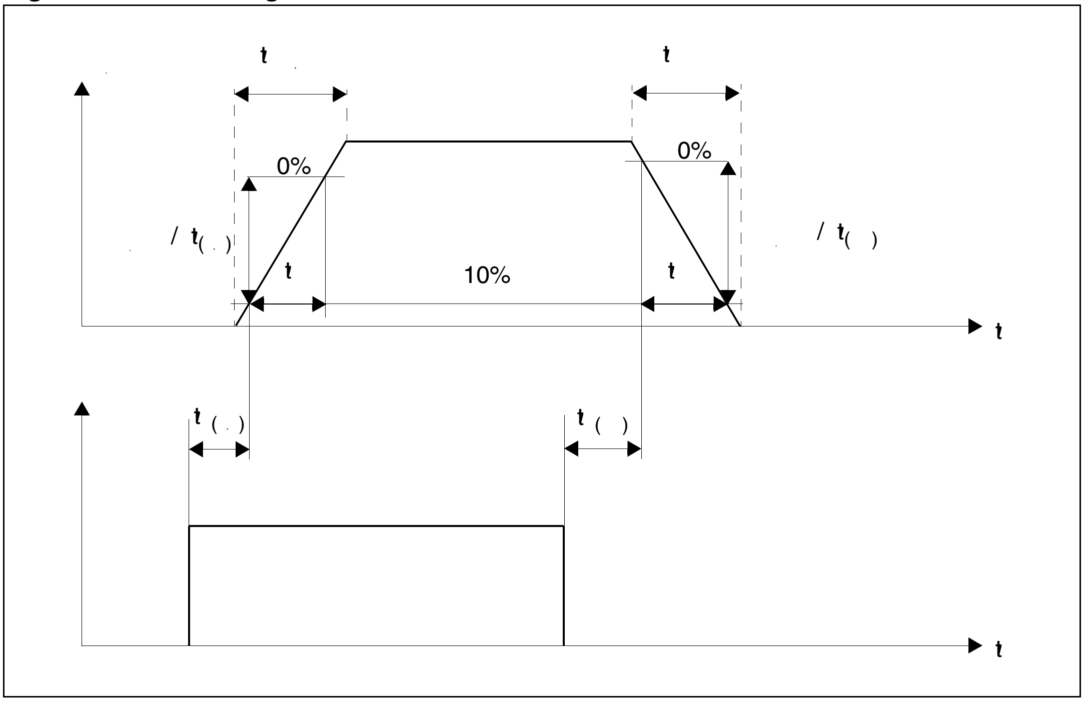


Figure 9. Output voltage drop limitation

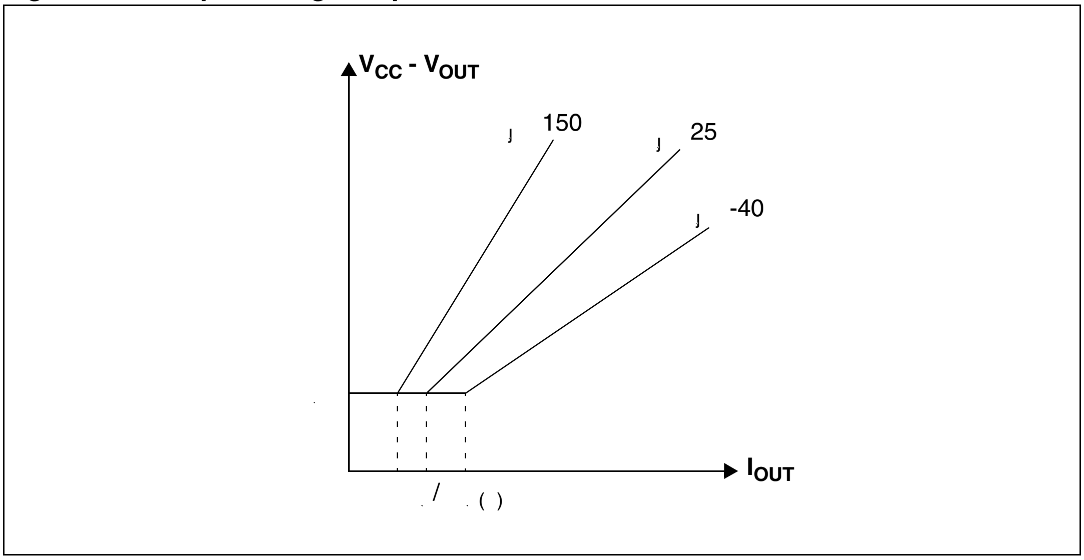


Table 11. Electrical transient requirements

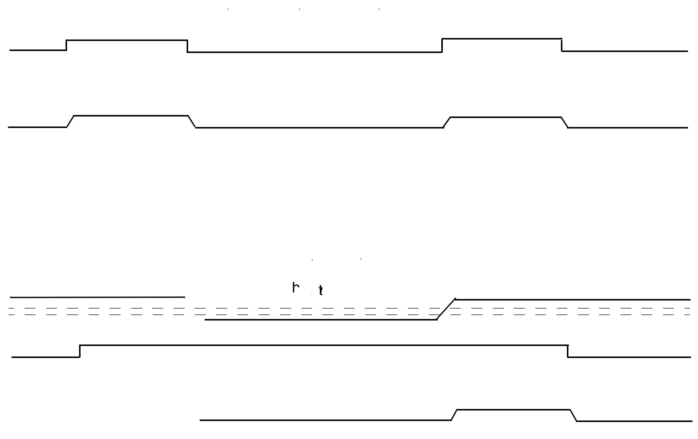
ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min	Max	
1	-75	-100	5000	0.5	5	2 , 10Ω
2	+37	+50	5000	0.2	5	50µ , 2Ω
3	-100	-150	[illegible]	0	100	0.1µ , 50Ω
3	+75	+100	[illegible]	0	100	0.1µ , 50Ω
4	-6	-7	1			100 , 0.01Ω
5 (2)	+65	+ 7	1			400 , 2Ω

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1		
2		
3		
3		
4		
5 (2)		

Class	Contents
	[illegible]
	[illegible]

1. [illegible] 13.5 [illegible] 5 .
2. [illegible] 40 [illegible]

Figure 10. Waveforms



[redacted]

Figure 11. Off state output current

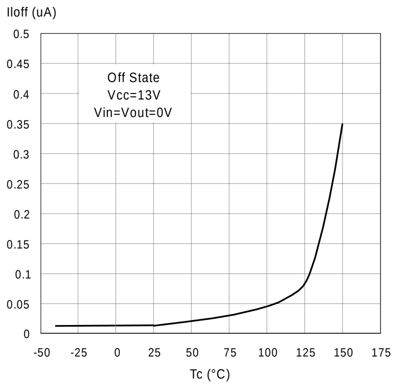


Figure 12. High level input current

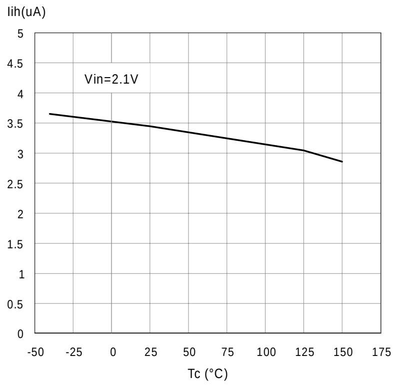


Figure 13. Input clamp voltage

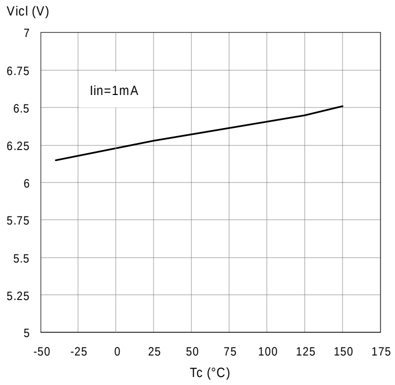


Figure 14. Input high level

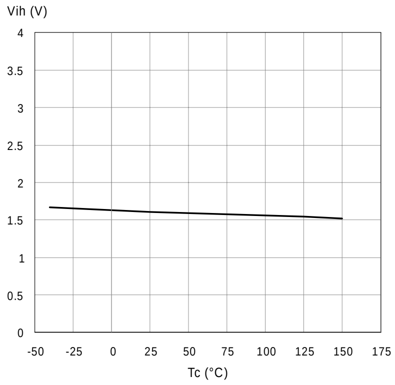


Figure 15. Input low level

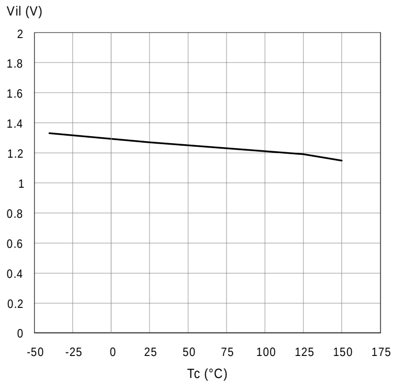


Figure 16. Input hysteresis voltage

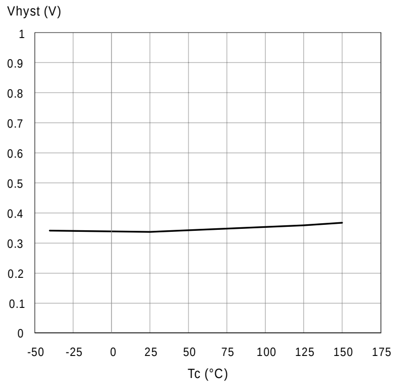


Figure 17. On state resistance vs T_{case}

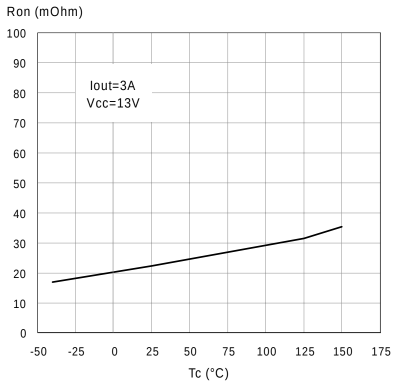


Figure 18. On state resistance vs V_{CC}

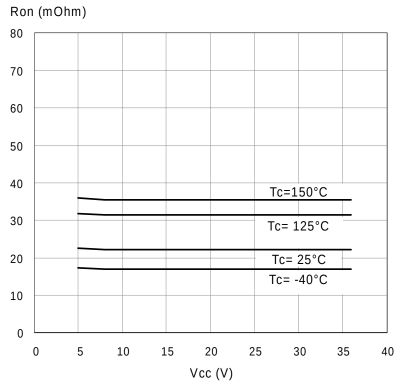


Figure 19. Undervoltage shutdown

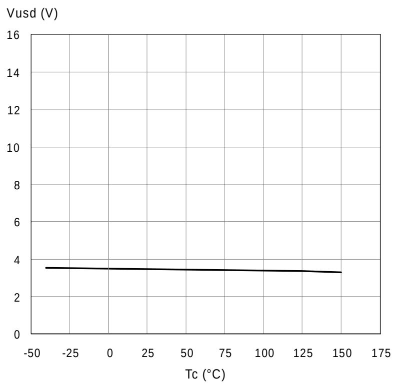


Figure 20. I_{LIMH} vs T_{case}

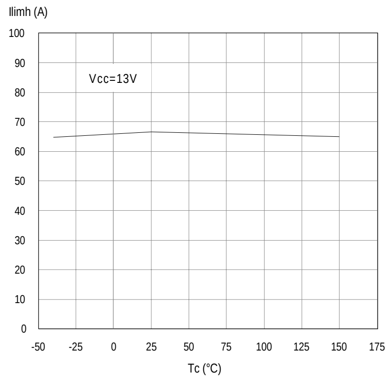


Figure 21. Turn-on voltage slope

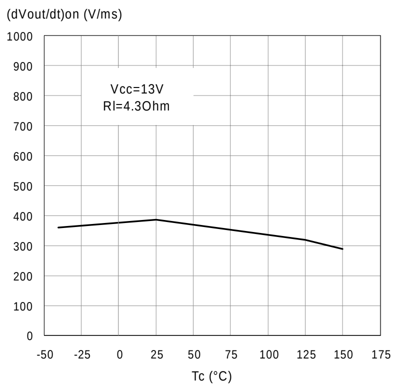


Figure 22. Turn-off voltage slope

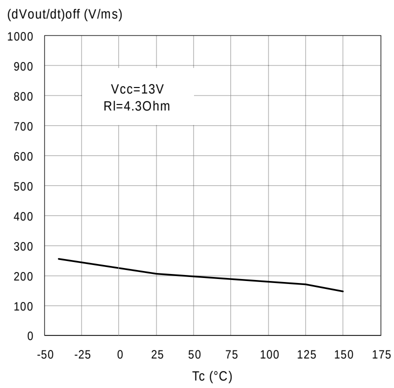


Figure 23. CS_DIS high level voltage

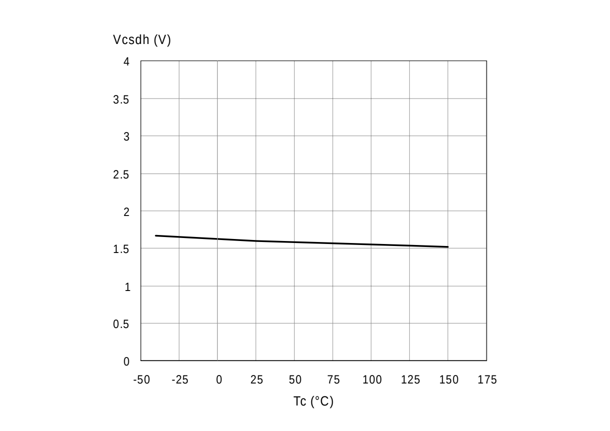


Figure 24. CS_DIS low level voltage

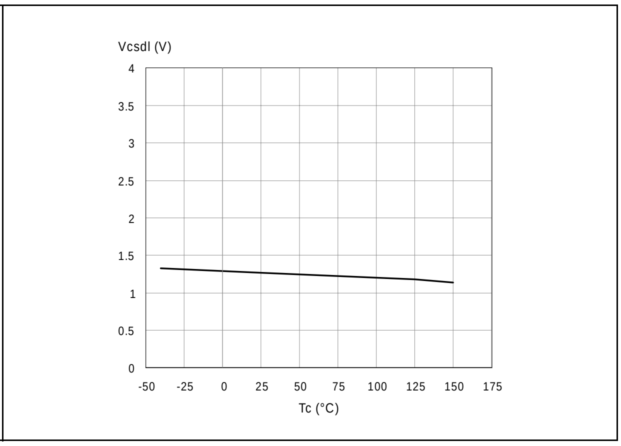
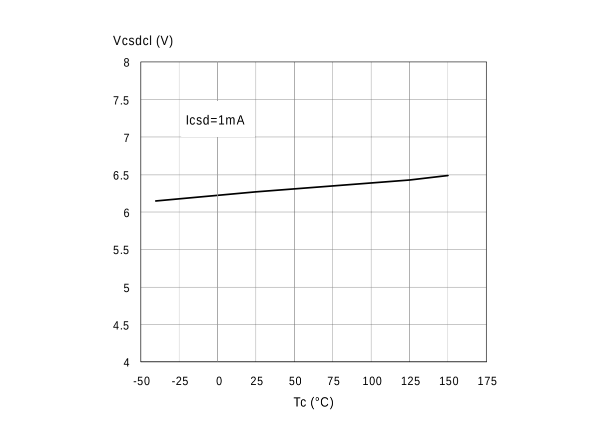
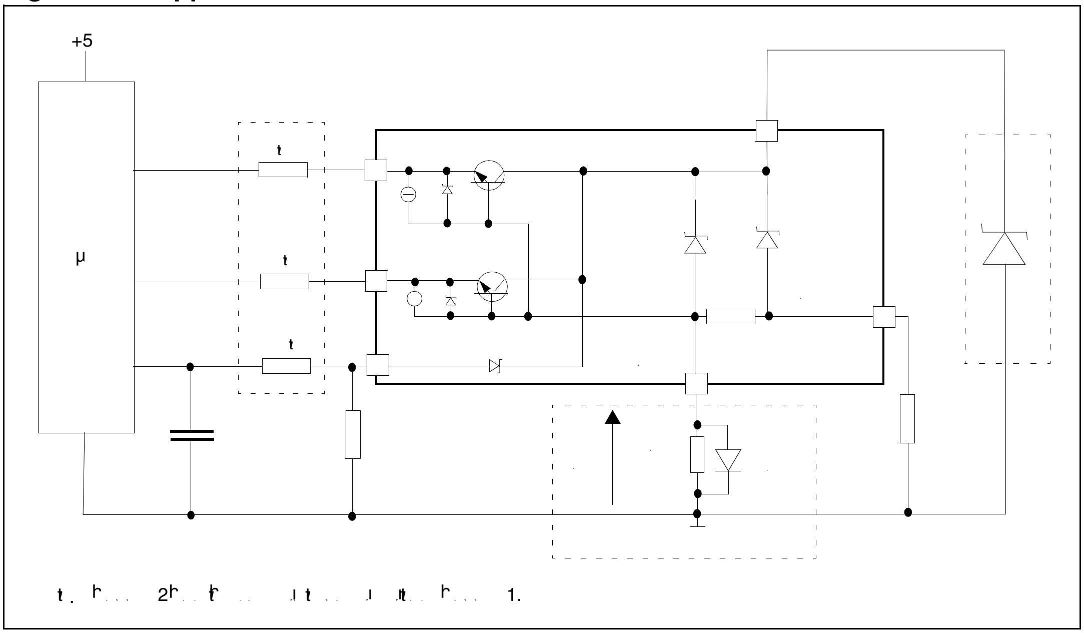


Figure 25. CS_DIS clamp voltage



3 Application information

Figure 26. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: Resistor in the ground line (R_{GND} only)

1. ≤ 600 / ((.))
2. ≥ (-) / (-)

0

$(-\ )^2 /$

(1),

[illegible] 2.

3.1.2 Solution 2: Diode (D_{GND}) in the ground line

[illegible] (j600 [illegible])

3.2 Load dump protection

[illegible] 7637-2 2004 [illegible]

3.3 µC I/Os protection

[illegible]

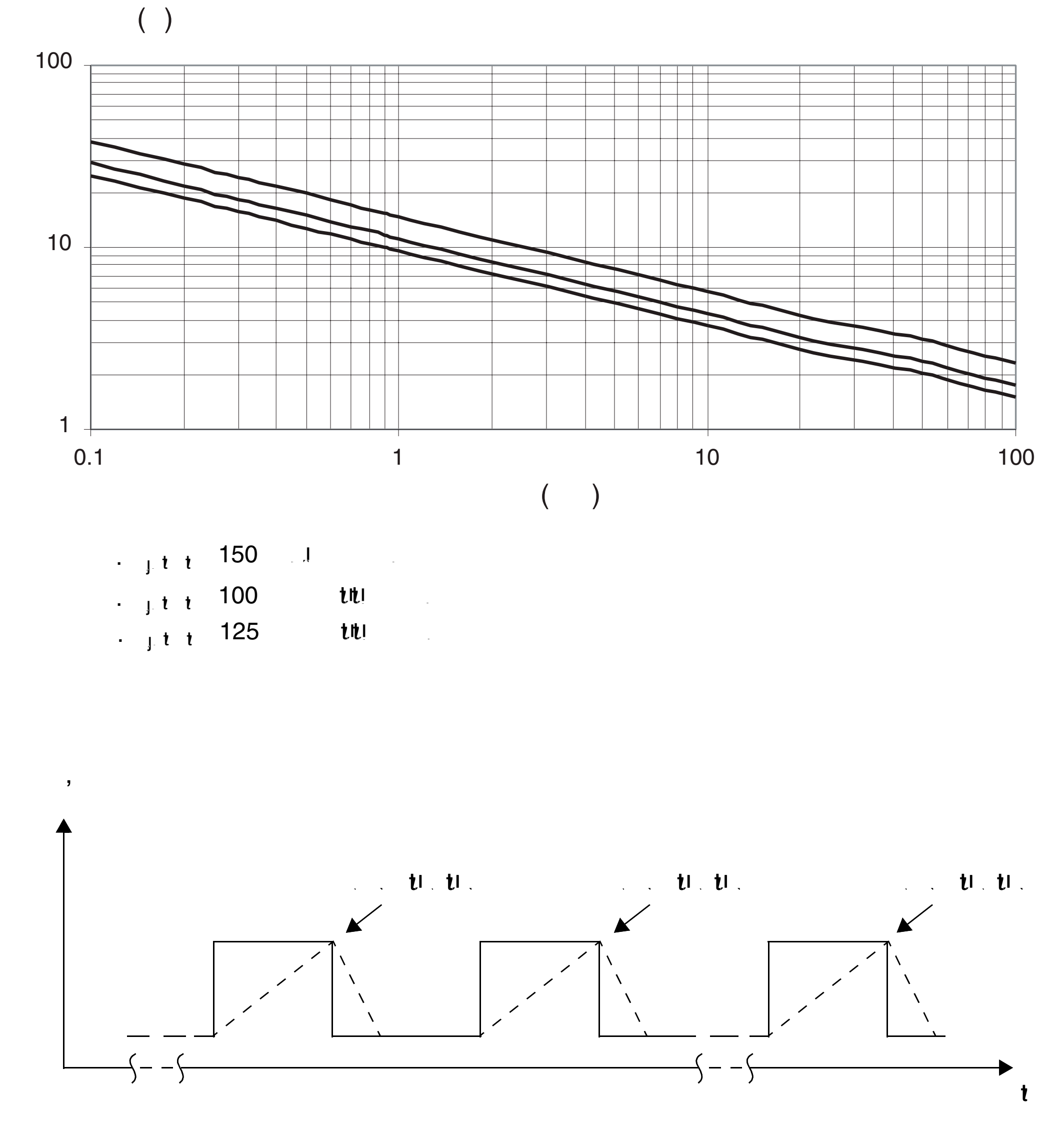
-100 [illegible] ≥ 20 [illegible] ≥ 4.5

5 Ω ≤ [illegible] ≤ 65 Ω

[illegible] 10 Ω, [illegible] 10

3.4 Maximum demagnetization energy (V_{CC} = 13.5V)

Figure 27. Maximum turn off current versus inductance (for each channel)



Note: *Values are generated with $R_L = 0\Omega$*

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and thermal data

4.1 PowerSSO-24™ thermal data

Figure 28. PowerSSO-24™ PC board

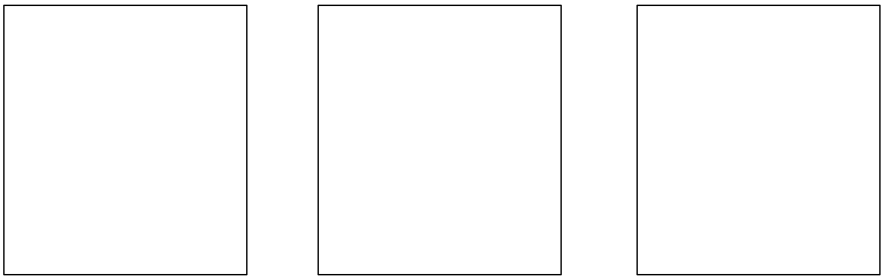


Figure 29. $R_{thj-amb}$ vs PCB copper area in open box free air condition (with one channel ON)

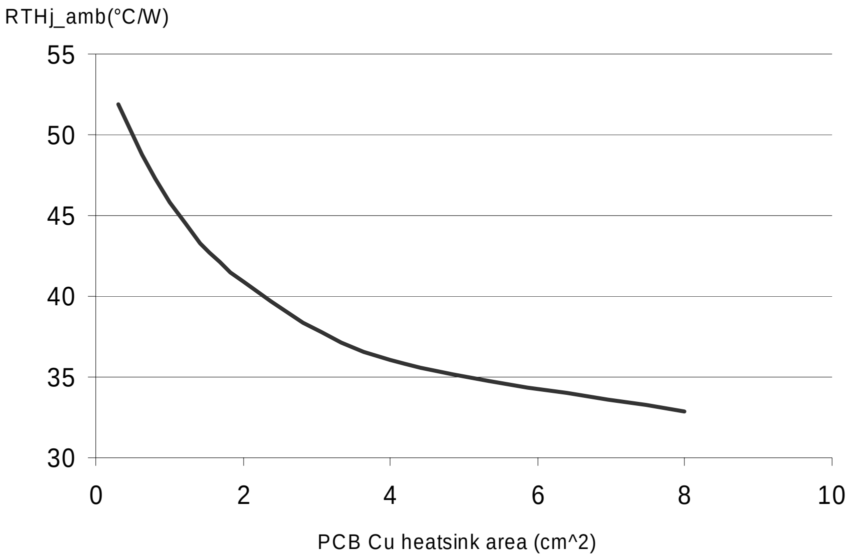


Figure 30. PowerSSO-24™ thermal impedance junction to ambient single pulse (with one channel ON)

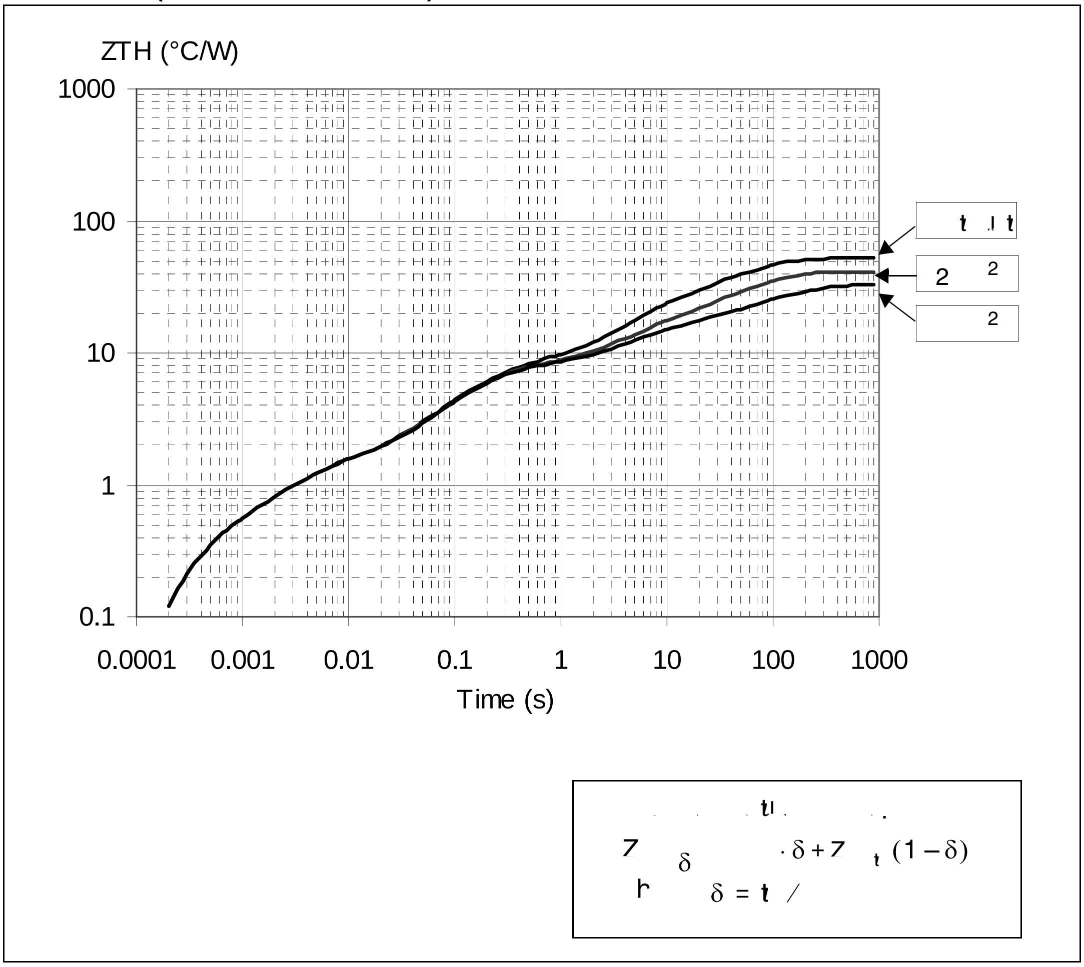


Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24™(1)

1. . . . . . . Table 12

Table 12. Thermal parameters

Area/Island (cm^2)	Footprint	2	8
1 (/)	0.2		
2 (/)	0.		
3 (/)	6		
4 (/)	7.7		
5 (/)			
6 (/)	2	17	10
7 (/)	0.2		
(/)	0.		
1 (. /)	0.001		
2 (. /)	0.003		
3 (. /)	0.025		
4 (. /)	0.75		
5 (. /)	1	4	
6 (. /)	2.2	5	17
7 (. /)	0.001		
(. /)	0.003		

5 Package and packing information

5.1 ECOPACK® packages

[illegible]

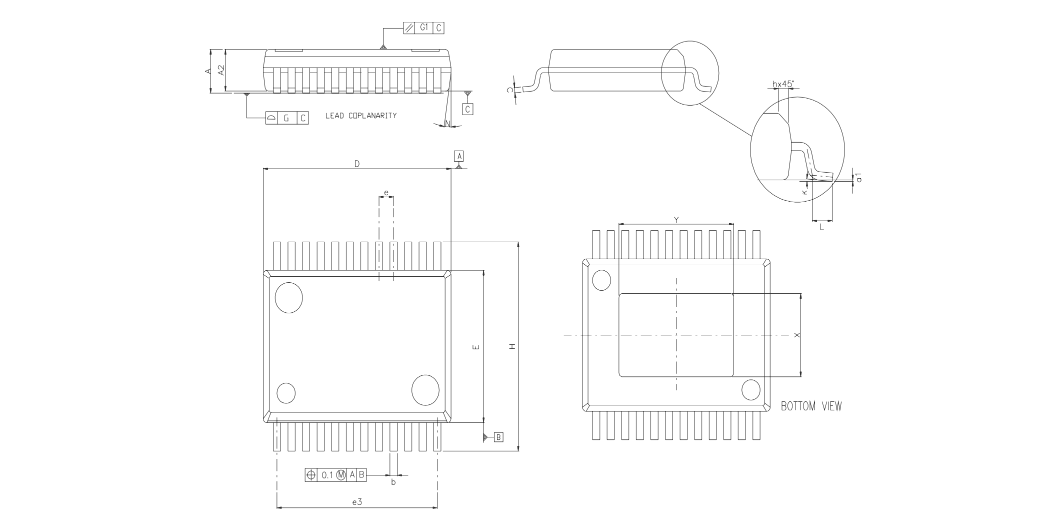
[illegible]

5.2 Package mechanical

Table 13. PowerSSO-24™ mechanical data

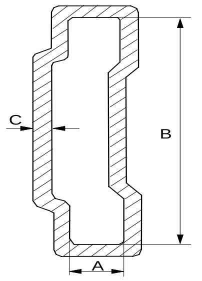
Symbol	Millimeters		
	Min	Typ	Max
[illegible]	1.		2.22
2	1.		2.15
1	0		0.07
[illegible]	0.34	0.4	0.46
[illegible]	0.23		0.32
[illegible]	10.2		10.4
[illegible]	7.4		7.6
[illegible]		0.	
3		.	
[illegible]			0.1
1			0.06
[illegible]	10.1		10.5
[illegible]			0.4
[illegible]	0.55		0. 5
[illegible]			10
[illegible]	3.		4.3
[illegible]	6.1		6.5

Figure 32. PowerSSO-24™ package dimensions



5.3 Packing information

Figure 33. PowerSSO-24™ tube shipment (no suffix)



Base Qty	4
Bulk Qty	1225
Tube length (±0.5)	532
A	3.5
B	13.
C (±0.1)	0.6

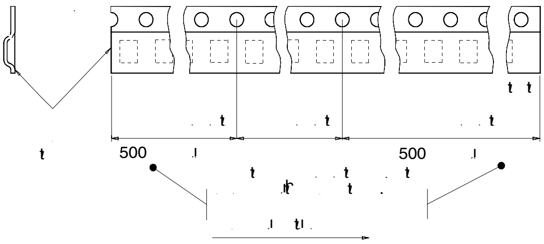
Figure 34. PowerSSO-24™ tape and reel shipment (suffix "TR")

REEL DIMENSIONS

Base Qty	1000
Bulk Qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

TAPE DIMENSIONS

Tape width	**W**	24
Tape Hole Spacing	**P0 (±0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (±0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.1)**	11.5
Compartment Depth	**K (max)**	2. 5
Hole Spacing	**P1 (±0.1)**	2



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
16- [illegible] -2007	1	[illegible]
23- [illegible] -2007	2	*Table 9: Current sense (8V < VCC < 16V)* [illegible]
2 [illegible] - [illegible] -2007	3	*Protection* [illegible]

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